On page 47, line 2, delete "Figure 8" and substitute --Figure 8a--.

On page 47, line 5, delete "from left to right" and substitute -- from right to left--.

On page 47, line 8, delete "right" and substitute --left--.

On page 47, line 9, delete the first "left" and substitute --right--.

On page 49, line 22, delete "primay" and substitute --primary--.

On page 54, line 13, delete "70" and substitute --69--.

On page 56, line 2, delete "Figurell" and substitute --Figure 11--.

On page 60, line 10, after "147" insert --A, B--.

IN THE CLAIMS:

Kindly **cancel** claims 1-150, without prejudice.

Kindly **add** the following claims:

151. A system comprising:

a first integrated circuit device coupled to an external signal line, the first integrated circuit device including:

output driver circuitry to output data onto the external signal line wherein:

the output driver circuitry outputs a first portion of data in response to a rising edge transition of an external clock signal; and

the output driver circuitry outputs a second portion of data in response to a falling edge transition of the external clock signal; and

a second integrated circuit device coupled to the external signal line, the second integrated circuit device including:

output driver circuitry to output data onto the external signal line wherein:

the output driver circuitry outputs a first portion of data in response to a rising edge transition of the external clock signal; and

the output driver circuitry outputs a second portion of data in response to a falling edge transition of the external clock signal.

152. The system of claim 151 further including a clock generator coupled to a second external signal line to generate the external clock signal, wherein the first and second integrated circuit devices are each coupled to the second external signal line.

3 ~~153~~. The system of claim 1 ~~151~~ wherein the first and second integrated circuit devices each include a clock alignment circuit coupled to the output driver circuitry.

4 ~~154~~. The system of claim 3 ~~153~~ wherein each clock alignment circuit is a delay lock loop circuit to generate an internal clock signal, and wherein the output driver circuitry outputs data in response to the internal clock signal.

5 ~~155~~. The system of claim 1 ~~151~~ wherein the first and second integrated circuit devices each further include:

multiplexer circuitry coupled to the output driver circuitry, wherein:

in response to a first transition of the external clock signal, the multiplexer circuitry couples the first portion of data to an input of the output driver circuitry; and

in response to a second transition of the external clock signal, the multiplexer circuitry couples the second portion of data to the input of the output driver circuitry.

6 ~~156~~. The system of claim 5 ~~155~~ wherein the first and second integrated circuit devices each further include a clock alignment circuit to generate a first internal clock signal, and wherein the multiplexer circuitry couples the first portion of data to the

A2

A

input of the output driver circuitry in response to the first internal clock signal.

7 6
157. The system of claim 156 wherein the clock alignment circuit generates a second internal clock signal, and wherein the multiplexer circuitry couples the second portion of data to the input of the output driver circuitry in response to the second internal clock signal.

8 1
158. The system of claim 151 wherein both the rising edge transition of the external clock signal and the falling edge transition of the external clock signal transpire during a first clock cycle of the external clock signal.

9 1
159. The system of claim 151 wherein both the rising and falling edge transitions of the external clock signal each include a voltage swing of less than one volt.

10 1
160. The system of claim 151 wherein the first and second integrated circuit devices each further include:

input receiver circuitry to sample data from the external signal line wherein:

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the input receiver circuitry samples a first portion of data in response to a rising edge transition of the external clock signal; and

the input receiver circuitry samples a second portion of data in response to a falling edge transition of the external clock signal.

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~~16~~. A system comprising:

a first integrated circuit device coupled to an external signal line, the first integrated circuit device including:

output driver circuitry to output data onto the external signal line wherein:

the output driver circuitry outputs a first portion of data synchronously with respect to a rising edge transition of an external clock signal; and

the output driver circuitry outputs a second portion of data synchronously with respect to a falling edge transition of the external clock signal; and

a second integrated circuit device coupled to the external signal line, the second integrated circuit device including:

input receiver circuitry to sample data from the external signal line wherein:

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the input receiver circuitry samples the first portion of data synchronously with respect to the rising edge transition of the external clock signal; and

the input receiver circuitry samples the second portion of data synchronously with respect to the falling edge transition of the external clock signal.

12 11
~~162~~. The system of claim ~~161~~ further including a clock generator coupled to a second external signal line to generate the external clock signal, wherein the first and second integrated circuit devices receive the external clock signal.

13 11
~~163~~. The system of claim ~~161~~ wherein the first integrated circuit device further includes a clock alignment circuit to receive the external clock signal and to generate an internal clock signal, wherein the output driver circuitry outputs data in response to the internal clock signal.

14 11
~~164~~. The system of claim ~~161~~ wherein the first integrated circuit device further includes:

multiplexer circuitry coupled to the output driver circuitry, wherein:

in response to a first transition of the external clock signal, the multiplexer circuitry couples the first portion of data to an input of the output driver circuitry; and

in response to a second transition of the external clock signal, the multiplexer circuitry couples the second portion of data to the input of the output driver circuitry.

15 ~~165~~. The system of claim 11 ~~161~~ wherein both the rising edge transition of the external clock signal and the falling edge transition of the external clock signal transpire during a first clock cycle of the external clock signal.

16 ~~166~~. The system of claim 11 ~~161~~ wherein both the rising and falling edge transitions of the external clock signal include voltage swings of less than one volt.

17 ~~167~~. The system of claim 11 ~~161~~ wherein the second integrated circuit further includes a clock alignment circuit to receive the external clock signal and to generate an internal clock signal, wherein the input receiver circuitry on the second integrated circuit device samples data in response to the internal clock signal.

168. ~~An integrated circuit device comprising:~~

output driver circuitry to output data onto a first external signal line wherein:

the output driver circuitry outputs a first portion of data in response to a rising edge transition of a first external clock signal and the output driver circuitry outputs a second portion of data in response to a falling edge ~~transition of the first external clock signal.~~

169. The integrated circuit device of claim ~~168~~ further including input receiver circuitry to sample data from a second external signal line wherein:

the input receiver circuitry samples a first portion of data in response to a rising edge transition of a second external clock signal; and

the input receiver circuitry samples a second portion of data in response to a falling edge transition of the second external clock signal.

170. The integrated circuit device of claim ~~169~~ further including a clock alignment circuit to generate a first internal clock signal, and wherein the input receiver circuitry samples the first portion of data in response to the first internal clock signal.

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~~171~~. The ~~system~~ of claim ~~170~~ wherein the clock alignment circuit generates a second internal clock signal, and the input receiver samples the second portion of data in response to the second internal clock signal.

~~172. The integrated circuit device of claim 168 wherein the clock alignment circuit generates an internal clock signal, and the output driver circuitry outputs data in response to the internal clock signal.~~

23 18

~~173~~. The integrated circuit device of claim ~~168~~ further including input receiver circuitry to sample data from the first external signal line wherein:

the input receiver circuitry samples a first portion of data in response to a rising edge transition of the first external clock signal; and

the input receiver circuitry samples a second portion of data in response to a falling edge transition of the first external clock signal.

24 18

~~174~~. The integrated circuit device of claim ~~168~~ further including:

multiplexer circuitry coupled to the first output driver circuitry, wherein:

in response to a first transition of the first external clock signal, the multiplexer circuitry couples the first portion of data to an input of the first output driver circuitry; and

in response to a second transition of the first external clock signal, the multiplexer circuitry couples the second portion of data to the input of the first output driver circuitry.

25 ~~175~~. The integrated circuit device of claim ~~174~~ 24 further including a clock alignment circuit to generate a first internal clock signal using the first external clock signal, wherein the multiplexer circuitry couples the first portion of data to the input of the first output driver circuitry in response to the first internal clock signal.

26 ~~176~~. The integrated circuit device of claim ~~175~~ 25 wherein the clock alignment circuit generates a second internal clock signal, and wherein the multiplexer circuitry couples the second portion of data to the input of the first output driver circuitry in response to the second internal clock signal.

177. The integrated circuit device of claim 176 further including a clock alignment circuit coupled to the first external